IN THE CLAIMS

Please amend the specification as follows:

1-19 (Canceled)

20. (Currently Amended) A method of fabricating a memory array, the method comprising:

forming from a single unbonded substrate a number of access transistors separated by trenches, each access transistor formed in a pillar of semiconductor material that extends outwardly from the single unbonded substrate wherein each access transistor includes, in order, a first source/drain region, a body region and a second source/drain region formed vertically thereupon;

filling the trenches with a polysilicon layer, the polysilicon layer having a top surface below a top surface of the body region;

forming a nitride layer over the access transistors and the polysilicon layer;

removing first portion of the nitride layer and the entire polysilicon layer to form a plurality of bridges, each of the bridges including second portion of the nitride layer, each of the bridges extending through a column of access transistors;

forming a trench capacitor in ~~a trench~~ the trenches, wherein a first plate of the trench capacitor is integral with the first source/drain region of the access transistor, wherein the trench capacitor is formed directly on the single unbonded substrate;

forming a number of word lines in ~~a number of~~ the trenches that separate adjacent rows of access transistors, wherein each trench includes two word lines with a gate of each word line interconnecting alternate access transistors on opposite sides of the trench;

forming a number of bit lines that interconnect second source/drain regions of selected access transistors.

21. (Previously Presented) The method of claim 20, wherein forming a trench capacitor further includes forming a second plate that surrounds the first plate.

22. (Previously Presented) The method of claim 20, and further comprising forming a contact that couples a second plate of the trench capacitor to an underlying layer.

23. (Previously Presented) The method of claim 20, where forming a trench capacitor comprises forming a second plate that forms a grid pattern in a layer of material such that the grid surrounds each of the pillars that form the access transistors.

24. (Previously Presented) The method of claim 20, wherein forming a trench capacitor comprises depositing poly-silicon in crossing row and column isolation trenches formed around the pillars that define the access transistors.

25. (Currently Amended) A method of fabricating a memory array, the method comprising:

epitaxially forming a first conductivity type first source/drain region layer on an unbonded substrate;

epitaxially forming a second conductivity type body region layer on the first source/drain region layer;

forming a first conductivity type second source/drain region layer on the body region layer;

forming a plurality of substantially parallel column isolation trenches extending through the second source/drain region layer, the body region layer, and the first source/drain region layer, thereby forming column bars between the column isolation trenches;

filling the column isolation trenches with a polysilicon layer, the polysilicon layer having a top surface below a top surface of the body region layer;

forming a nitride layer over the column bars and the polysilicon layer;

removing a first portion of the nitride layer and the entire polysilicon layer to form

~~forming~~ a plurality of substantially parallel row isolation trenches, orthogonal to the column isolation trenches, extending to substantially the same depth as the column isolation trenches, thereby forming an array of vertical access transistors for the memory array, wherein

the removing the first portion of the nitride layer the entire polysilicon layer also forms a plurality of bridges orthogonal to the column isolation trenches, each of the bridges including a second portion of the nitride layer, each of the bridges extending through a column of vertical access transistors;

filling the row and column isolation trenches with a conductive material to a level that does not exceed the lower level of the body region so as to provide a common plate for capacitors of memory cells of the memory array, wherein the capacitors are formed directly on the unbonded substrate;

forming two conductive word lines in each row isolation trenches that selectively interconnect alternate vertical access transistors on opposite sides of the row isolation trench; and

forming bit lines that selectively interconnect the second source/drain regions of the vertical access transistors on each column.

26. (Previously Presented) The method of claim 25, wherein forming the first conductivity type source/drain region layer on the unbonded substrate comprises forming the first conductivity type first source/drain region layer outwardly from the unbonded substrate to a distance sufficient for the first source/drain region layer to also function as a first plate of the capacitor for each memory cell in the array.

27. (Original) The method of claim 20, wherein the memory array comprises memory cells each occupying an area of 4F2, wherein F is a minimum feature size.

28. (Original) The method of claim 20, wherein the first source/drain region is N+ doped.

29. (Original) The method of claim 28, including forming the first source/drain region to a thickness of approximately 3.5 micrometers.

30. (Original) The method of claim 28, wherein the body region is P- doped.

31. (Original) The method of claim 30, including forming the body region by epitaxial growth of single-crystalline P- silicon to a thickness of approximately 0.5 microns.

32. (Original) The method of claim 30, wherein the second source/drain region is N+ doped.

33. (Original) The method of claim 32, including forming the second source/drain region by implanting the N+ dopant to a depth of approximately 0.1 microns.

34. (Original) The method of claim 25, wherein the memory array comprises memory cells each occupying an area of 4F2, wherein F is a minimum feature size.

35. (Original) The method of claim 25, wherein the first source/drain region is N+ doped.

36. (Original) The method of claim 35, including forming the first source/drain region to a thickness of approximately 3.5 micrometers.

37. (Original) The method of claim 35, wherein the unitary body region is P- doped.

38. (Original) The method of claim 37, including forming the body region by epitaxial growth of single-crystalline P- silicon to a thickness of approximately 0.5 microns.

39. (Original) The method of claim 37, wherein the second source/drain region is N+ doped.

40. (Original) The method of claim 39, including forming the second source/drain region by implanting the N+ dopant to a depth of approximately 0.1 microns.

41. (Currently Amended) A method of forming an array of memory cells, the method comprising:

forming using a single unbonded substrate a plurality of isolated vertical access transistors separated by trenches, the isolated vertical access transistors comprising in order outward from the single unbonded substrate, a first source drain region, a body region and a second source/drain region, wherein the separation of trenches is such that the area occupied by each memory cell is 4F2, wherein F is a minimum feature size;

filling the trenches with a polysilicon layer, the polysilicon layer having a top surface below a top surface of the body region;

forming a nitride layer over the isolated vertical access transistors and the polysilicon layer;

removing a first portion of the nitride layer and the entire polysilicon layer to form a plurality of bridges, each of the bridges including a second portion of the nitride layer, each of the bridges extending through a column of isolated vertical access transistors;

forming a trench capacitor for each memory cell, wherein a portion of the first source/drain region serves as a first plate of the capacitor, the trench capacitor is formed directly on the single unbonded substrate;

forming two word lines in select trenches, with a gate of each word line interconnecting alternate isolated vertical access transistors on opposite sides of the trench; and

forming bit lines that interconnect select second source/drain regions.

42. (Original) The method of claim 41, wherein the first source/drain region is N+ doped.

43. (Original) The method of claim 41 including forming the first source/drain region to a thickness of approximately 3.5 micrometers.

44. (Original) The method of claim 42, wherein the body region is P- doped.

45. (Original) The method of claim 43, including forming the body region by epitaxial growth of single-crystalline P- silicon to a thickness of approximately 0.5 microns.

46. (Original) The method of claim 44, wherein the second source/drain region is N+ doped.

47. (Original) The method of claim 46, including forming the second source/drain region by implanting the N+ dopant to a depth of approximately 0.1 microns.

48. (Previously Presented) The method of claim 41, wherein forming the trench capacitor further includes forming a second plate that surrounds the first plate.

49. (Previously Presented) A method of forming an array of memory cells, the method comprising:

forming with a single unbonded substrate a first layer of a first conductivity type of single crystalline silicon, a second layer of a second conductivity type of single crystalline silicon, and a third layer of the first type of single crystalline silicon atop the second layer;

selectively etching through the third through first layers and partially into the single unbonded substrate so as to form a plurality of trenches and pillars spaced apart such that the surface area occupied by each memory cell is 4F2, wherein F is a minimum feature size;

filling the trenches with a polysilicon layer, the polysilicon layer having a top surface below a top surface of the second layer;

forming a nitride layer over the pillars and the polysilicon layer;

removing a first portion of the nitride layer and the entire polysilicon layer to form a plurality of bridges, each of the bridges including a second portion of the nitride layer, each of the bridges extending through a column of pillars;

filling the trenches with a conductive material so as to provide for a common plate for capacitors associated with each memory cell, such that a portion of the first layer in each pillar serves as a plate for the capacitor, wherein the capacitors are formed directly on the single unbonded substrate;

electrically interconnecting select pillars by word lines electrically coupled to the second layer of the select pillars, wherein each of the trenches includes two word lines; and

electrically interconnecting the select pillars by bit lines electrically coupled to the third layer of the select pillars.

50. (Original) A method according to claim 46, wherein the first conductivity type is N+ and the second conductivity type is P-.

51. (Currently Amended) A method of fabricating an array of memory cells, the method comprising:

forming, using a single unbonded substrate, spaced apart access transistors isolated by trenches, each access transistor comprising in order from the single unbonded substrate outward, an N+ - doped first source/drain region, a P- doped body region and an N+ -doped second source/drain region;

filling the trenches with a polysilicon layer, the polysilicon layer having a top surface below a top surface of the body region;

forming a nitride layer over the access transistors and the polysilicon layer;

removing a first portion of the nitride layer and the entire polysilicon layer to form a plurality of bridges, each of the bridges including a second portion of the nitride layer, each of the bridges extending through a column of the access transistors;

forming capacitors in the trench corresponding to each access transistor, wherein a portion of the N+ -doped first source/drain region adjacent the single unbonded substrate serves as a plate for the capacitor corresponding to each access transistor, wherein the capacitors are formed directly on the single unbonded substrate; and

electrically connecting the access transistors in a manner that allows for an electrical charge to be accessed or stored in each capacitor via the corresponding access transistor, wherein each of the trenches includes two word lines selectively connected to the access transistors.

52. (Currently Amended) A method according to claim 51, wherein electrically connecting the access transistors includes:

forming a number of bit lines that interconnect second source/drain regions of selected access transistors.

53. (Currently Amended) A method of forming a memory device having an array of memory cells and a minimum feature size F, comprising:

forming using a single unbonded substrate a plurality of vertical access transistors separated by trenches and laid out in a substantially checker-board pattern such that the memory cells occupy an area of 4F2, wherein the formation of the vertical access transistors consists of forming a first source/drain region of a first dopant type, forming a body region of a second dopant type atop the first source/drain region, and forming a second source/drain region of a second dopant type atop the body region;

filling the trenches with a polysilicon layer, the polysilicon layer having a top surface below a top surface of the body region;

forming a nitride layer over the vertical access transistors and the polysilicon layer;

removing a first portion of the nitride layer and the entire polysilicon layer to form a plurality of bridges, each of the bridges including a second portion of the nitride layer, each of the bridges extending through a column of vertical access transistors;

forming a capacitor in the trenches by lining the trench with a gate oxide, and then filling the trench with polysilicon of the first type so as to surround a portion of the first source/drain region such that the surrounded portion of the first source/drain region serves as a first plate of the capacitor and the polysilicon in the trench serves as a second plate of the capacitor, wherein the capacitor is formed directly on the single unbonded substrate; and

electrically connecting the vertical access transistors via bit lines and word lines so as to provide the capability of accessing a charge stored in one or more of the capacitors or providing a charge thereto, wherein each of the trenches includes two word lines selectively connected to the vertical access transistors.

54. (Original) The method of claim 53, further including connecting the word lines to a word line decoder and the bit lines to a bit line decoder to provide selective access to the memory cells.

55. (Currently Amended) A method of forming an electronic device having an array of memory cells and a minimum feature size F, comprising:

forming with a single unbonded substrate a plurality of spaced apart access transistors each comprising in order outward from the single unbonded substrate, a first layer of N+ dopant serving as first source/drain, a second layer of P- dopant serving as a body region and a third layer of N+ dopant serving as a second source/drain region;

wherein the forming of the access transistors includes forming trenches therebetween so as to provide a memory cell area of 4F2;

filling the trenches with a polysilicon layer, the polysilicon layer having a top surface below a top surface of the body region;

forming a nitride layer over the access transistors and the polysilicon layer;

removing a first portion of the nitride layer and the entire polysilicon layer to form a plurality of bridges, each of the bridges including a second portion of the nitride layer, each of the bridges extending through a column of access transistors;

forming, for each access transistor, a capacitor in the trenches by filling the trench with a thin layer of oxide and polysilicon, such that a portion of the first source/drain, the oxide layer and the polysilicon respectively serve as a first plate, a dielectric, and a second plate for the capacitor, wherein the capacitor is formed directly on the single unbonded substrate;

electrically connecting the access transistors with word lines and bit lines, wherein each of the trenches includes two word lines selectively connected to the access transistors;

connecting the word lines to a word line decoder;

connecting the bit lines to a bit line decoder;

operatively connecting the word line and bit line decoders to an address buffer; and

interfacing the address buffer to an electronic system via address lines.

56. (Original) The method of claim 55, wherein the electronic system is a microprocessor.

57. (New) A method comprising:

growing a first layer over a substrate, the first layer including single crystalline silicon;

growing a middle layer over the first layer, the middle layer including single crystalline silicon;

growing a second layer over the middle layer, the second layer including single crystalline silicon;

depositing a pad layer over the second layer;

performing an etching process to form a plurality of parallel column trenches and a plurality of column bars interleaved with the column trenches, wherein the etching process includes etching the pad layer, etching the second layer, etching the middle layer, etching the first layer, and etching a portion of the substrate, and wherein each of the column bars includes a portion of the substrate, a portion of the first layer, a portion of the middle layer, a portion of the second layer, and a portion of the pad layer;

filling the column trenches with a polysilicon layer;

etching the polysilicon layer to a level below a top surface of the portion of the first layer in each of the column bars;

depositing a nitride layer over the column bars and the polysilicon layer;

planarizing the nitride layer to a level even with a surface of the portion of the pad layer of each of the column bars;

forming a photoresist layer over the nitride layer and the portion of the pad layer of each of the column bars, the photoresist layer having masked portion and openings, the each of the openings extending orthogonal to the column trenches;

etching the column bars, the nitride layer, and the polysilicon layer through the openings, wherein the etching exposes the polysilicon layer at the openings, and wherein the portion of the pad layer of each of the column bars under the masked portion and the nitride layer under the masked portion remain intact;

isotropically etching the polysilicon layer to form a plurality of row trenches orthogonal to the column trenches, a plurality of pillars arranged in column pillars parallel to the column trenches and arranged in rows pillars parallel to the row trenches, and a plurality bridges, each of the bridges connecting pillars in a column pillar, wherein each of the pillars includes a portion of the substrate, a first pillar portion formed by a part of the first layer, a middle pillar portion formed by a part of the middle layer, a second pillar portion formed by a part of the second layer, and a pad pillar portion formed by a part of the pad layer, wherein each of the bridges includes the nitride layer and the part of the pad layer in each pillar within a column pillar, and wherein each of the bridges has a bottom surface below a level of the top surface of the part of the first layer.

forming a dielectric on the substrate and on side walls of the first pillar portion of each of the pillars;

forming a conductive layer on the column trenches and the row trenches, wherein a surface of the conductive layer is at a level even with a level of the bottom surface of each of the bridges;

forming an insulation layer on the surface of the conductive layer;

forming an insulation layer on exposed side walls of each of the pillars, wherein the exposed side walls are side walls above the surface of the conductive layer;

forming at least one word line in each of the row trenches; and

forming a plurality of bit lines, each of the bit lines connecting the second pillar portion of each pillar in a column pillars.

58. (New) A method comprising:

forming a first layer over a substrate, the first layer having a first conductivity type material;

forming a middle layer over the first layer, the middle layer having a second conductivity type material;

forming a second layer over the middle layer, the second layer having a first conductivity type material;

forming a first nitride layer over the second layer;

forming a plurality of parallel column trenches and a plurality of column bars interleaved with the column trenches;

forming a polysilicon layer in the column trenches, the polysilicon layer having a top surface below a top surface of the portion of the first layer in each of the column bars;

forming a second nitride layer over the column bars and the polysilicon layer, the second nitride layer having a top surface even with a top surface of the portion of the first nitride layer of each of the column bars;

removing a portion of the second nitride layer and the entire polysilicon layer to form a plurality of row trenches orthogonal to the column trenches, a plurality of pillars arranged in column pillars parallel to the column trenches and arranged in rows pillars parallel to the row trenches, and a plurality bridges, each of the bridges connecting pillars in a column pillar, wherein each of the pillars includes a portion of the substrate, a first pillar portion formed by a part of the first layer, a middle pillar portion formed by a part of the middle layer, a second pillar portion formed by a part of the second layer, and a nitride pillar portion formed by a part of the first nitride layer, wherein each of the bridges includes a top surface even with the top even with the top surface of the part of the first nitride layer of each of the pillars, and wherein each of the bridges includes a bottom surface below a level of the top surface of the part of the first layer of each of the pillars.

forming a dielectric on the substrate and on side walls of the first pillar portion of each of the pillars;

forming a conductive layer on the column trenches and the row trenches, wherein a surface of the conductive layer is at a level even with a level of the bottom surface of each of the bridges;

forming an insulation layer on the surface of the conductive layer;

forming an insulation layer on exposed side walls of each of the pillars, wherein the exposed side walls are side walls above the surface of the conductive layer;

forming a pair of word lines in each of the row trenches; and

forming a plurality of bit lines, each of the bit lines connecting the second pillar portion of each pillar in a column pillars.

59. (New) A method comprising:

forming on a substrate a plurality of parallel column trenches and a plurality of column bars interleaved with the column trenches, wherein each of the column bars includes and a portion of the substrate, a first layer, a middle layer, a second layer, and a pad layer;

forming a polysilicon layer in the column trenches, the polysilicon layer having a top surface below a top surface of the portion of the first layer in each of the column bars;

forming a nitride layer over the column bars and the polysilicon layer, the nitride layer having a top surface even with a top surface of the portion of the pad layer of each of the column bars;

removing a portion of the nitride layer the entire polysilicon layer to form a plurality of row trenches orthogonal to the column trenches, a plurality of pillars arranged in column pillars parallel to the column trenches and arranged in rows pillars parallel to the row trenches, and a plurality bridges, each of the bridges connecting pillars in a column pillar, wherein each of the pillars includes, a portion of the substrate, a the first pillar portion formed by part of the first layer, a middle pillar portion formed by a part of the middle layer, a second pillar portion formed by a part of the second layer, and a pad portion formed by a part of the pad layer, wherein each of the bridges includes a top surface even with the top even with the top surface of the part of the pad layer of each of the pillars, and wherein each of the bridges includes a bottom surface below a level of the top surface of the part of the first layer of each of the pillars.

forming a dielectric on the substrate and on side walls of the first pillar portion of each of the pillars;

forming a conductive layer on the column trenches and the row trenches, wherein a surface of the conductive layer is at a level even with a level of the bottom surface of each of the bridges, wherein the first pillar portion, the middle pillar portion, and the second pillar portion form a source, a drain, and a body region of a vertical transistor, wherein the conductive layer and the first pillar portion of each of the pillars form a plurality of trench capacitors;

forming an insulation layer on the surface of the conductive layer;

forming an insulation layer on exposed side walls of each of the pillars, wherein the exposed side walls are side walls above the surface of the conductive layer;

forming a pair of word lines in each of the row trenches; and

forming a plurality of bit lines, each of the bit lines connecting the second pillar portion of each pillar in a column pillars.